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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,447	06/05/2001	Shunpei Yamazaki	740756-2322	4413

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,447	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-123* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *See Continuation Sheet* is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims allowed are 47-52,59,60,63,64,67,68,71,72,82-93,96,97,100-103,110,111,114,115,118,119,122 and 123.
Continuation of Disposition of Claims: Claims rejected are 43-46,53-58,61,62,65,66,69,70,73-81,94,95,98,99,104-109,112,113,116,117,120 and 121.

DETAILED ACTION

This office action is in response to the filing of the amendment on 11 May 2005. Claims 43-123 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 43, 44, 53-56, 69, 70, 73, 79, 94, 95, 104-107, 120 and 121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. (6,472,256) in view of Kawaguchi et al. (4,940,934).

Referring to claims 43, 44, 73, 79, 94 and 95, Zhang et al. disclose a method of manufacturing a display panel for an active matrix type device where an interlayer insulating film (44) is formed to cover a plurality of thin film transistors (TFT 11 and 31) provided on an insulating surface (41) (Fig. 11A; col. 14, lines 10-15); forming contact holes (44S, 64S, 44D, and 64D) in the interlayer insulating film (44) (Fig. 11B; col. 14, lines 15-21); forming a plurality of connecting wirings (45S, 65S, 45D and 65D) respectively connected to source regions or drain regions (41S, 61S, 41D and 61D) of the thin film transistors (TFT 11 and 31) through the contact holes (44S, 64S, 44D, and 64D) (Fig. 11D; col. 14, lines 23-36); forming a conductive film (47); making the plurality of thin film transistors (TFT 11 and 311) in an on state, wherein an on state is defined by

a predetermined electric potential is applied to one of a source region and a drain region of a TFT, the state of the TFT is defined as being on if a desired potential can be applied to the other (col. 4, lines 54-61); and forming a plurality of pixel electrodes (47) by patterning the conductive film to be electrically connected to the plurality of thin film transistors (TFT 11), respectively (Fig. 12C; col. 14, line 65 thru col. 15, line 12).

Zhang et al. do not disclose forming a measurement wiring in contact with the insulating surface, measuring a value of electric current flowing in the measurement wiring, and judging whether or not the plurality of thin film transistors are defective from the value prior to forming a plurality of pixel electrodes.

Kawaguchi et al. disclose a method of manufacturing a display panel where a plurality of thin film transistors (C_{11}, C_{12}, C_{21}) is connected to a measurement wiring (Fig. 1-2B; col. 4, lines 6-26); measuring a value of electric current flowing in the measurement wiring, and judging whether or not the plurality of thin film transistors (C_{11}, C_{12}, C_{21}) are defective from the value (col. 4, lines 27-32); and forming a plurality of pixel electrodes (D_{11}, D_{12}, D_{21}) to be electrically connected to the plurality of thin film transistors (C_{11}, C_{12}, C_{21}) after the judging (Fig. 4; col. 3, lines 12-25).

Since Zhang et al. and Kawaguchi et al. are both from the same field of endeavor, a method of manufacturing a display panel, the purpose disclosed by Kawaguchi et al. would have been recognized in the pertinent art of Zhang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Zhang et al. by measuring a value of electric current flowing in a measurement wiring, and judging whether or not the plurality of thin film

transistors are defective as taught by Kawaguchi to determine the number of defective pixels prior to assembling the display panel (col. 1, lines 25-37).

Referring to claims 53-56, 98, 99 and 104-107, Zhang et al. disclose the method forming a display panel for an active matrix type device (col. 4, lines 47-54).

"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

Referring to claims 69, 70, 120 and 121, Zhang et al. disclose using the display panel as a notebook type personal computer (col. 1, lines 15-25).

Claims 45, 46, 74-76, 98 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. in view of Kawaguchi et al. as applied to claims 43, 44 and 73 above, and further in view of Yamazaki et al. (6,274,887).

Zhang et al. in view of Kawaguchi et al. disclose the subject matter claimed above except laminating EL layers and an opposing electrode on pixel electrodes.

Yamazaki et al. disclose a method of manufacturing a display panel for an active matrix type device where an interlayer insulating film (7) is formed to cover a plurality of thin film transistors (4102) provided on an insulating surface (4101) (col. 31, lines 30-63); forming contact holes in the interlayer insulating film; forming a plurality of connecting wirings (4135) respectively connected to source regions or drain regions of the thin film transistors (4102) through the contact holes; forming a conductive film; making the plurality of thin film transistors (4102) in an on state; and forming a plurality of pixel electrodes (4143) by patterning the conductive film to be electrically connected to the plurality of thin film transistors (4103) (col. 32, lines 28-31).

Referring to claims 45, 46, 76, 98 and 99, Yamazaki et al. further disclose laminating EL layers (4145) and an opposing electrode (4147) on pixel electrodes (4143) (col. 33, lines 9-17).

Since Zhang et al. and Yamazaki et al. are both from the same field of endeavor, a method of manufacturing a display panel, the purpose disclosed by Yamazaki et al. would have been recognized in the pertinent art of Zhang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify Zhang et al. by laminating EL layers and an opposing electrode on pixel electrodes as taught by Yamazaki et al. to increase efficiency (col. 33, liens 20-34).

Referring to claims 74 and 75, Kawaguchi et al. disclose switching thin film transistors, a power source supply line, and a pixel electrode electrically connected (col. 1, lines 37-56).

Claims 57, 58, 61, 62, 80, 81, 108, 109, 112 and 113 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. in view of Kawaguchi et al. further in view of Nakase et al. (5,760,855).

Zhang et al. in view of Kawaguchi et al. disclose the subject matter claimed above except a source signal line driver circuit, a gate signal line driver circuit, and a controller are attached to the display panel.

Nakase et al. disclose a method of manufacturing a display panel where a plurality of thin film transistors (5) are provided on an insulating surface (1); making the plurality of thin film transistors (5) in an on state; and forming a plurality of pixel electrodes to be electrically connected to the plurality of thin film transistors (5) (col. 5, line 64 thru col. 6, line 5).

Referring to claims 57, 58, 108 and 109, Nakase et al. disclose attaching a source signal line driver circuit (4) and a gate signal line driver circuit (3) to the display panel (col. 5, lines 51-67).

Since Zhang et al. and Nakase et al. are both from the same field of endeavor, a method of manufacturing a display panel, the purpose disclosed by Nakase et al. would have been recognized in the pertinent art of Zhang et al. Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify Zhang et al. by attaching a source signal line driver circuit, a gate signal line driver circuit, and a controller to the display panel as taught by Nakase et al. to prevent static induced damages (col. 3, lines 14-22).

Referring to claims 61, 62, 112 and 113, Kawaguchi et al. disclose attaching a controller to the display panel (col. 1, lines 38-56).

Referring to claims 80 and 81, Kawaguchi et al. disclose measuring a value of electric current flowing in the measurement wiring, and judging whether or not the plurality of thin film transistors are defective from the value (col. 6, lines 33-49).

Claims 65, 66, 116 and 117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. in view of Kawaguchi et al. as applied to claims 43, 44, 73-75, 94 and 95 above, and further in view of Hiroki (6,729,922).

Zhang et al. in view of Kawaguchi et al. disclose the subject matter claimed above except attaching a source signal line driver circuit, a gate signal line driver circuit, a controller, and a microcomputer are attached to the display panel.

Hiroki discloses a method of manufacturing a display panel for an active matrix type device where an interlayer insulating film is formed to cover a plurality of thin film transistors provided on an insulating surface (5056); forming contact holes in the interlayer insulating film (5056); forming a plurality of connecting wirings (5057) respectively connected to source regions or drain regions of the thin film transistors through the contact holes; forming a conductive film; making the plurality of thin film transistors in an on state (Fig. 6A); and forming a plurality of pixel electrodes (5063) by

patterning the conductive film to be electrically connected to the plurality of thin film transistors (Fig. 6B; col. 14, lines 7-58).

Referring to claims 65, 66, 116 and 117, Hiroki discloses attaching a source signal line driver circuit (1802), a gate signal line driver circuit (1803), a controller (1804), and a microcomputer (1805) are attached to the display panel (col. 21, lines 39-67).

Since Zhang et al. and Hiroki are both from the same field of endeavor, a method of manufacturing a display panel for an active matrix type device, the purpose disclosed by Hiroki would have been recognized in the pertinent art of Zhang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Zhang et al. by attaching a source signal line driver circuit, a gate signal line driver circuit, a controller, and a microcomputer are attached to the display panel as taught by Hiroki to inspect the device for defects (col. 3, lines 36-40).

Claims 77 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. in view of Kawaguchi et al. further in view of Nakase et al. as applied to claims 74 and 75 above, and further in view of Yamazaki et al.

Zhang et al. in view of Kawaguchi et al. further in view of Nakase et al. disclose the subject matter claimed above except laminating EL layers and an opposing electrode on pixel electrodes.

Yamazaki et al. disclose a method of manufacturing a display panel for an active matrix type device where an interlayer insulating film (7) is formed to cover a plurality of thin film transistors (4102) provided on an insulating surface (4101) (col. 31, lines 30-

63); forming contact holes in the interlayer insulating film; forming a plurality of connecting wirings (4135) respectively connected to source regions or drain regions of the thin film transistors (4102) through the contact holes; forming a conductive film; making the plurality of thin film transistors (4102) in an on state; and forming a plurality of pixel electrodes (4143) by patterning the conductive film to be electrically connected to the plurality of thin film transistors (4103) (col. 32, lines 28-31).

Referring to claims 77 and 78, Yamazaki et al. further disclose laminating EL layers (4145) and an opposing electrode (4147) on pixel electrodes (4143) (col. 33, lines 9-17).

Since Zhang et al. and Yamazaki et al. are both from the same field of endeavor, a method of manufacturing a display panel, the purpose disclosed by Yamazaki et al. would have been recognized in the pertinent art of Zhang et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Zhang et al. by laminating EL layers and an opposing electrode on pixel electrodes as taught by Yamazaki et al. to increase efficiency (col. 33, liens 20-34).

Allowable Subject Matter

Claims 47-52, 59, 60, 63, 64, 67, 68, 71, 72, 82-93, 96, 97, 100-103, 110, 111, 114, 115, 118, 119, 122 and 123 allowed.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest forming an inspection conductive film electrically connected to all of a plurality of pixel electrodes electrically connected to

a plurality of thin film transistors respectively, measuring a value of electric current flowing in a measurement wiring, and judging whether or not the plurality of thin film transistors and the plurality of pixel electrodes are defective from the value; and removing said inspection conductive film.

Response to Arguments

Applicant's arguments with respect to claims 43-123 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Inoue et al. (5,693,959) disclose a display panel for an active matrix type device where an interlayer insulating film is formed to cover a plurality of thin film transistors provided on an insulating surface; forming contact holes in the interlayer insulating film; forming a plurality of connecting wirings respectively connected to source regions or drain regions of the thin film transistors through the contact holes; forming a conductive film; making the plurality of thin film transistors in an on state; and forming a plurality of pixel electrodes by patterning the conductive film to be electrically connected to the plurality of thin film transistors.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Michael Trinh
Primary Examiner
Act SPE